

The structure depicted in FIG. 2 is completed by depositing a suitable insulating material, such as TiO_x , Si_3N_4 , or other suitable barrier insulation material, over the memory cell. A thick layer of interlevel dielectric is formed, and suitable contacts for the source, gate and drain regions are installed. Referring now to FIGS. 3a and 3b, the construction and structure of a two transistor memory cell having a stacked gate unit will be described. In this instance, the structure is formed on a silicon substrate 40 which has an oxide layer 42 formed thereover. Regions for the source, drain, and gate may be formed at this step of the method, or may be formed later. In any event, a layer of n⁺ polysilicon 44 is deposited, preferably by CVD which, with oxide layer 42, forms a MOS capacitor 46. A lower metal layer, or electrode 48, is then formed over the n⁺ polysilicon layer 44, as previously described. A top plan view of lower metal layer 48 is depicted in FIG. 3b.